WHAT IS CLAIMED IS:

1. A method for detecting metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising:

annealing the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material;

measuring a tunneling voltage of the dielectric material; and

determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured tunneling voltage.

2. The method of claim 1, wherein the annealed dielectric material is substantially free of damage.

3. The method of claim 1, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature, and wherein the metal contamination comprises one type of metal contamination.

4. The method of claim 1, wherein the metal contamination comprises at least two types of metal contamination.

5. The method of claim 1, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of less than approximately 1100 °C.

6. The method of claim 1, wherein the metal contamination comprises copper, and wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of approximately 350 °C to approximately 500 °C.

7. The method of claim 1, wherein the metal contamination comprises copper, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes.

8. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing the charge comprises using a non-contact corona charging technique.

9. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein the deposited charge comprises approximately $1x10^{-6}$ C/cm^2 to approximately $1x10^{-4}$ C/cm^2 for positive tunneling voltage.

10. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein the deposited charge comprises approximately $-1x10^{-6}$ C/cm^2 to approximately $-1x10^{-4}$ C/cm^2 for negative tunneling voltage.

11. The method of claim 1, wherein measuring the tunneling voltage comprises:

depositing a charge on an upper surface of the dielectric material;

waiting for a predetermined period of time after depositing a charge on an upper surface of the dielectric material; and

determining the tunneling voltage.

12. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing a charge on an upper surface of the dielectric material comprises depositing the charge on predetermined regions of the upper surface of the dielectric material.

13. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing the charge on the upper surface of the dielectric material comprises depositing the charge on a portion of the upper surface or on substantially the entire upper surface.

14. The method of claim 1, wherein measuring the tunneling voltage of the dielectric material comprises using a non-contact work function measurement technique.

15. The method of claim 1, further comprising comparing the tunneling voltage of the dielectric material to a tunneling voltage of a reference dielectric material, wherein the reference dielectric material is substantially free of metal contamination.

16. The method of claim 1, further comprising comparing the tunneling voltage of the dielectric material to a tunneling voltage of a reference dielectric material, wherein the reference dielectric material comprises a predetermined level of at least one type of metal contamination, and wherein at least the one type of metal contamination is predetermined.

17. The method of claim 1, further comprising determining a tunneling field of the dielectric material, wherein the tunneling field is a function of the tunneling voltage, the method further comprising comparing the tunneling field of the dielectric material to a tunneling field of a reference dielectric material, wherein the reference dielectric material is substantially free of contamination.

18. The method of claim 1, further comprising determining a tunneling field of the dielectric material, wherein the tunneling field is a function of the tunneling voltage, the method further comprising comparing the tunneling field of the dielectric material to a tunneling field of a reference dielectric material, wherein the reference dielectric material comprises a predetermined level of at least one type of metal contamination, and wherein at least the one type of metal contamination is predetermined.

19. The method of claim 1, wherein determining a characteristic of the metal contamination in the dielectric material comprises comparing the tunneling voltage of the dielectric material to a tunneling voltage of a reference dielectric material.

20. The method of claim 1, further comprising determining a tunneling field of the dielectric material, wherein the tunneling field is a function of the tunneling voltage.

21. The method of claim 1, further comprising determining a tunneling field of the dielectric material, wherein determining the tunneling field comprises subtracting a tunneling voltage of a reference dielectric material from the tunneling voltage of the dielectric material.

22. The method of claim 1, wherein the characteristic of the metal contamination further comprises a function of a temperature of the annealing of the semiconductor substrate.

23. The method of claim 1, wherein the characteristic of the metal contamination further comprises a function of an amount of the deposited charge.

24. The method of claim 1, wherein determining the characteristic of the metal contamination in the dielectric material comprises determining a characteristic of at least two types of metal contamination in the dielectric material.

25. The method of claim 1, wherein determining a characteristic of the metal contamination in the dielectric material comprises determining a characteristic of at least one type of metal contamination in a portion of the dielectric material, and wherein the portion of the dielectric material comprises a locally contaminated region of the dielectric material.

26. The method of claim 1, further comprising measuring the tunneling voltage of the dielectric material at more than one position on the semiconductor substrate, determining a tunneling field of the dielectric material at each measurement position, and determining the characteristic of at least one type of metal contamination at each measurement position.

27. The method of claim 26, further comprising generating a plot of the determined tunneling field as a function of measurement position.

28. The method of claim 27, further comprising comparing the generated plot of the determined tunneling field as a function of measurement position to a plot of a predetermined tunneling field as a function of measurement position.

29. The method of claim 28, wherein the predetermined tunneling field is representative of a range of acceptable levels of at least one type of metal contamination, and wherein the acceptable levels of the metal contamination do not substantially hinder the performance of a semiconductor device formed on the semiconductor substrate.

30. The method of claim 1, further comprising annealing the semiconductor substrate subsequent to depositing the charge on an upper surface of the semiconductor substrate.

31. The method of claim 30, further comprising heating the semiconductor substrate to an annealing temperature of less than approximately 120 °C.

32. The method of claim 30, further comprising heating the semiconductor substrate to an annealing temperature of less than approximately 120 °C, wherein the metal contamination comprises copper, and wherein the dielectric material comprises silicon dioxide.

33. The method of claim 1, further comprising generating electrical stress in the dielectric material and heating the semiconductor substrate subsequent to generating the electrical stress in the dielectric material.

34. The method of claim 33, wherein generating electrical stress comprises using a non-contact corona charging technique, and wherein the electrical stress comprises approximately -1×10^{-3} C/cm^2 to approximately $+1 \times 10^{-3}$ C/cm^2.

35. The method of claim 33, wherein heating the semiconductor substrate comprises heating the semiconductor substrate to a temperature of approximately 50 °C to approximately 120 °C.

36. The method of claim 33, wherein heating the semiconductor substrate comprises heating the semiconductor substrate for a period of time of approximately one minute to approximately thirty minutes.

37. The method of claim 1, further comprising determining a presence of particulate contamination on the dielectric layer, wherein the presence of particulate contamination is a function of the measured tunneling voltage.

38. The method of claim 37, further comprising flowing a gas across an upper surface of the dielectric material as a charge is deposited onto the dielectric material.

39. The method of claim 38, wherein the gas has a moisture content, and wherein the moisture content of the gas is greater than a moisture content of air surrounding the semiconductor substrate.

40. The method of claim 38, wherein the gas comprises ammonia.

41. The method of claim 1, wherein the dielectric material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

42. The method of claim 1, wherein the semiconductor substrate comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

43. The method of claim 1, wherein the metal contamination comprises copper.

44. The method of claim 1, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum.

45. The method of claim 1, further comprising comparing the tunneling voltage to a set of data, wherein the set of data comprises tunneling voltages associated with a characteristic of metal contamination.

46. The method of claim 1, further comprising

re-annealing the semiconductor substrate subsequent to measuring the tunneling voltage; and

re-measuring the tunneling voltage of the dielectric material.

47. A method for increasing degradation of a dielectric material resulting from metal contamination, comprising:

generating electrical stress in the dielectric material, wherein the dielectric material is disposed upon a semiconductor substrate; and

heating the semiconductor substrate subsequent to generating electrical stress in the dielectric material.

48. The method of claim 47, wherein generating electrical stress in the dielectric material comprises using a non-contact corona charging technique.

49. The method of claim 47, wherein the electrical stress comprises approximately -1×10^{-3} C/cm^2 to approximately $+1 \times 10^{-3}$ C/cm^2.

50. The method of claim 47, wherein heating the semiconductor substrate comprises heating the semiconductor substrate to a temperature of approximately 50 °C to

approximately 120 °C.

51. The method of claim 47, wherein heating the semiconductor substrate comprises heating the semiconductor substrate for a period of time of approximately one minute to approximately thirty minutes.

52. The method of claim 47, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum.

53. The method of claim 47, wherein the metal contamination comprises copper.

54. The method of claim 47, wherein the dielectric material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

55. A method for determining a characteristic of metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising:

annealing the semiconductor substrate prior to depositing a charge on an upper surface of the dielectric material, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material;

depositing a charge upon the upper surface of the dielectric material;

annealing the semiconductor substrate subsequent to depositing a charge on the upper surface of the dielectric material;

measuring a tunneling voltage of the dielectric material; and

determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured tunneling voltage.

56. The method of claim 55, wherein annealing the semiconductor substrate prior to depositing the charge comprises heating the semiconductor substrate to an annealing temperature of less than approximately 1100 °C.

57. The method of claim 55, wherein the metal contamination comprises copper, and wherein annealing the semiconductor substrate prior to depositing the charge comprises heating the semiconductor substrate to an annealing temperature of approximately 350 °C to approximately 500 °C.

58. The method of claim 55, wherein the metal contamination comprises copper, wherein annealing the semiconductor substrate prior to depositing the charge comprises heating the semiconductor substrate for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes.

59. The method of claim 55, wherein annealing the semiconductor substrate subsequent to depositing the charge comprises heating the semiconductor substrate to an annealing temperature of less than approximately 120 °C.

60. The method of claim 55, wherein annealing the semiconductor substrate subsequent to depositing the charge comprises heating the semiconductor substrate to an annealing temperature of less than approximately 120 °C, wherein the metal contamination comprises copper, and wherein the dielectric material comprises silicon dioxide.

61. The method of claim 55, wherein the dielectric material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

62. The method of claim 55, wherein the semiconductor substrate comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

63. The method of claim 55, wherein the metal contamination comprises copper.

64. The method of claim 55, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum.

65. A method for detecting metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising:

annealing the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material;

measuring an electrical property of the dielectric material; and

determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured electrical property.

66. The method of claim 65, wherein the annealed dielectric material is substantially free of damage.

67. The method of claim 65, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature, and wherein the metal contamination comprises one type of metal contamination.

68. The method of claim 65, wherein the metal contamination comprises at least two types of metal contamination.

69. The method of claim 65, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of less than approximately 1100 °C.

70. The method of claim 65, wherein the metal contamination comprises copper, and wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of approximately 350 °C to approximately 500 °C.

71. The method of claim 65, wherein the metal contamination comprises copper, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes.

72. The method of claim 65, wherein measuring the electrical property comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing the charge comprises using a non-contact corona charging technique.

73. The method of claim 65, wherein measuring the electrical property comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing a charge on the upper surface of the dielectric material comprises depositing the charge on predetermined regions of the upper surface of the dielectric material.

74. The method of claim 65, wherein measuring the electrical property comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing

the charge on the upper surface of the dielectric material comprises depositing the charge on a portion of the upper surface or on substantially the entire upper surface.

75. The method of claim 65, wherein measuring the electrical property of the dielectric material comprises using a non-contact work function measurement technique.

76. The method of claim 65, further comprising comparing the electrical property of the dielectric material to an electrical property of a reference dielectric material, wherein the reference dielectric material is substantially free of metal contamination.

77. The method of claim 65, further comprising comparing the electrical property of the dielectric material to an electrical property of a reference dielectric material, wherein the reference dielectric material comprises a predetermined level of at least one type of metal contamination, and wherein at least the one type of metal contamination is predetermined.

78. The method of claim 77, further comprising determining a presence of at least one type of metal contamination in the dielectric material.

79. The method of claim 65, wherein measuring the electrical property of the dielectric material comprises depositing a charge on an upper surface of the semiconductor substrate, and wherein the deposited charge comprises an electric field of approximately a tunneling field of the dielectric material.

80. The method of claim 79, wherein the electric field comprises approximately 1 MV/cm to approximately 9 MV/cm for positive bias or approximately –1 MV/cm to approximately –9 MV/cm for negative bias, wherein the electrical property comprises a

surface voltage of the dielectric material, and wherein the surface voltage is a function of time.

81. The method of claim 65, wherein measuring the electrical property of the dielectric material further comprises determining a resistivity of the dielectric material, and wherein the characteristic of the metal contamination is a function of the resistivity of the dielectric material.

82. The method of claim 65, wherein the electrical property of the dielectric material comprises a flatband voltage.

83. The method of claim 65, wherein the electrical property of the dielectric material comprises an interface trap density.

84. The method of claim 65, wherein the electrical property of the dielectric material comprises a total dielectric charge.

85. The method of claim 65, wherein the characteristic of the metal contamination further comprises a function of a temperature of the annealing of the semiconductor substrate.

86. The method of claim 65, wherein the characteristic of the metal contamination further comprises a function of an amount of the deposited charge.

87. The method of claim 65, wherein determining the characteristic of the metal contamination in the dielectric material comprises determining a characteristic of at least two types of metal contamination in the dielectric material.

88. The method of claim 65, wherein determining a characteristic of the metal contamination in the dielectric material comprises determining a characteristic of at least one type of metal contamination in a portion of the dielectric material, and wherein the portion of the dielectric material comprises a locally contaminated region of the dielectric material.

89. The method of claim 65, further comprising measuring the electrical property of the dielectric material at more than one position on the semiconductor substrate, and determining the characteristic of at least one type of metal contamination at each measurement position.

90. The method of claim 89, further comprising generating a plot of the measured electrical property as a function of measurement position.

91. The method of claim 90, further comprising comparing the generated plot of the measured electrical property as a function of measurement position to a plot of a predetermined electrical property as a function of measurement position.

92. The method of claim 91, wherein the predetermined electrical property is representative of a range of acceptable levels of at least one type of metal contamination, and wherein the acceptable levels of the metal contamination do not substantially hinder the performance of a semiconductor device formed on the semiconductor substrate.

93. The method of claim 65, wherein the dielectric material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

94. The method of claim 65, wherein the semiconductor substrate comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

95. The method of claim 65, wherein the metal contamination comprises copper.

96. The method of claim 65, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum.

97. The method of claim 65, further comprising comparing the electrical property to a set of data, wherein the set of data comprises electrical properties associated with a characteristic of metal contamination, and wherein the set of data comprises data generated using one device configured to measure the electrical property of the dielectric material and to determine a characteristic of at least one type of metal contamination in the dielectric material.

98. The method of claim 65, further comprising

re-annealing the semiconductor substrate subsequent to measuring the electrical property; and

re-measuring the electrical property of the dielectric material.

99. A method for detecting metal contamination in a semiconductor substrate, comprising:

annealing the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the semiconductor substrate;

measuring a surface photo-voltage of the semiconductor substrate; and

determining a characteristic of the metal contamination in the semiconductor substrate, wherein the characteristic of the metal contamination is a function of the measured surface photo-voltage.

100. The method of claim 99, further comprising measuring a surface voltage of the semiconductor substrate prior to measuring the surface photo-voltage.

101. The method of claim 100, wherein the characteristic of the metal contamination further comprises a function of the measured surface voltage.

102. The method of claim 99, further comprising forming a dielectric material upon the semiconductor substrate prior to annealing the semiconductor substrate.

103. The method of claim 99, wherein measuring the surface photo-voltage comprises depositing a charge on an upper surface of the dielectric material, directing a pulse of light toward the semiconductor substrate, and determining the surface photo-voltage.

104. The method of claim 99, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature, and wherein the metal contamination comprises one type of metal contamination.

105. The method of claim 99, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature, and wherein the metal contamination comprises at least two types of metal contamination.

106. The method of claim 99, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of less than approximately 1100 °C.

107. The method of claim 99, wherein the metal contamination comprises copper, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of approximately 350 °C to approximately 500 °C.

108. The method of claim 99, wherein the metal contamination comprises copper, and wherein annealing the semiconductor substrate comprises heating the semiconductor substrate for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes.

109. The method of claim 99, further comprising rapidly cooling the semiconductor substrate subsequent to annealing the semiconductor substrate, wherein rapidly cooling the semiconductor substrate is effective to prevent diffusion of the metal contamination out of the semiconductor substrate.

110. The method of claim 99, further comprising depositing a charge on an upper surface of the semiconductor substrate using a non-contact corona charging technique.

111. The method of claim 99, further comprising depositing a charge on an upper surface of the semiconductor substrate, wherein the deposited charge comprises approximately $-1x10^{-4}$ C/cm^2 to approximately $1x10^{-4}$ C/cm^2, and wherein the deposited charge drives the semiconductor substrate to depletion.

112. The method of claim 99, further comprising depositing a charge on predetermined regions of an upper surface of the semiconductor substrate.

113. The method of claim 99, further comprising depositing a charge on a portion of an upper surface of the semiconductor substrate or on substantially an entire upper surface of the semiconductor substrate.

114. The method of claim 99, further comprising directing a pulse of light toward the semiconductor substrate, wherein an intensity of the light generates a surface photo-voltage within approximately 90 % of a saturation value of the surface photo-voltage.

115. The method of claim 99, further comprising comparing the surface photo-voltage of the semiconductor substrate to a surface photo-voltage of a reference semiconductor substrate, wherein the reference semiconductor substrate is substantially free of metal contamination.

116. The method of claim 99, further comprising comparing the surface photo-voltage of the semiconductor substrate to a surface photo-voltage of a reference semiconductor substrate, wherein the reference semiconductor substrate comprises a predetermined level of a least one type of metal contamination, and wherein at least the one type of metal contamination is predetermined.

117. The method of claim 116, further comprising determining a presence of at least one type of metal contamination in the semiconductor substrate.

118. The method of claim 99, further comprising determining a bulk minority carrier lifetime of the semiconductor substrate, wherein the bulk minority carrier lifetime of the semiconductor substrate comprises a function of the surface photo-voltage, and wherein the characteristic further comprises a function of the determined bulk minority carrier lifetime.

119. The method of claim 99, wherein measuring the surface photo-voltage of the semiconductor substrate comprises using a non-contact work function measurement technique.

120. The method of claim 99, wherein the characteristic of the metal contamination in the semiconductor substrate is a function of an annealing temperature.

121. The method of claim 99, wherein the characteristic of the metal contamination in the semiconductor substrate is a function of a corona field strength.

122. The method of claim 99, wherein determining a characteristic of the metal contamination in the semiconductor substrate comprises determining a characteristic of at least two types of metal contamination in the semiconductor substrate.

123. The method of claim 99, wherein determining a characteristic of the metal contamination in the semiconductor substrate comprises determining a level of the metal contamination in a portion of the semiconductor substrate, and wherein the portion of the semiconductor substrate comprises a locally contaminated region of the semiconductor substrate.

124. The method of claim 99, further comprising measuring the surface photo-voltage of the semiconductor substrate at more than one position on the semiconductor substrate, determining the surface photo-voltage of the semiconductor substrate at each measurement position, and determining the characteristic of the metal contamination at each measurement position.

125. The method of claim 124, further comprising generating a plot of the determined surface photo-voltage as a function of measurement position.

126. The method of claim 125, further comprising comparing the generated plot of the determined surface photo-voltage as a function of measurement position to a plot of predetermined surface photo-voltage as a function of measurement position.

127. The method of claim 126, wherein the predetermined surface photo-voltage is representative of a range of acceptable levels of at least one type of metal contamination, and wherein the acceptable levels of the metal contamination do not substantially hinder the performance of a semiconductor device formed on the semiconductor substrate.

128. The method of claim 99, wherein the semiconductor substrate comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

129. The method of claim 99, wherein the metal contaminant comprises copper.

130. The method of claim 99, wherein the metal contaminant comprises iron, chromium, cobalt, or aluminum.

131. The method of claim 99, further comprising comparing the surface photo-voltage to a set of data, wherein the set of data comprises surface photo-voltages associated with a characteristic of the metal contamination.

132. The method of claim 99, further comprising

re-annealing the semiconductor substrate subsequent to measuring the electrical property; and

re-measuring the electrical property of the dielectric material.

133. A system configured to measure a characteristic of metal contamination on a semiconductor topography during use, comprising:

an oven configured to anneal a semiconductor topography during use;

a device configured to deposit a charge on an upper surface of the semiconductor topography during use; and

a sensor configured to measure at least one electrical property of the charged upper surface of the semiconductor topography during use.

134. The system of claim 133, wherein the semiconductor topography comprises a semiconductor substrate.

135. The system of claim 133, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate.

136. The system of claim 133, wherein the oven is configured to heat the semiconductor topography to an anneal temperature of less than approximately 1100 °C.

137. The system of claim 133, wherein the oven is configured to drive the metal contamination into a semiconductor substrate of the semiconductor topography during use.

138. The system of claim 133, wherein the oven is configured to drive the metal

contamination into a dielectric material of the semiconductor topography during use.

139. The system of claim 133, wherein the device comprises a non-contact corona charging device.

140. The system of claim 133, wherein the device is configured to deposit a charge on predetermined regions of the semiconductor topography.

141. The system of claim 133, wherein the device is configured to deposit a charge on a portion of the semiconductor topography during use or on substantially the entire semiconductor topography during use.

142. The system of claim 133, wherein the sensor comprises a non-contact work function sensor.

143. The system of claim 133, further comprising a movable chuck configured to alter a position of the semiconductor topography under the device during use.

144. The system of claim 133, further comprising a robotic wafer handler configured to move the semiconductor topography during use.

145. The system of claim 133, further comprising a pre-aligner configured to alter a position of the semiconductor topography during use.

146. The system of claim 133, further comprising a cooling device configured to reduce a temperature of the semiconductor topography subsequent to annealing the semiconductor topography during use.

147. The system of claim 133, wherein the electrical property of the semiconductor topography comprises a tunneling voltage.

148. The system of claim 133, wherein the electrical property of the semiconductor topography comprises a surface voltage.

149. The system of claim 133, wherein the electrical property of the semiconductor topography comprises a surface voltage, and wherein the surface voltage is a function of time.

150. The system of claim 133, wherein the electrical property of the semiconductor topography comprises a surface photo-voltage of the semiconductor topography, and wherein the system further comprises an illumination system configured to direct a pulse of light toward the semiconductor substrate during use and a movable chuck configured to alter a position of the semiconductor topography under the illumination system during use.

151. The system of claim 133, further comprising an operating system, wherein the operating system is configured to monitor and control the oven, the device and the sensor during use, wherein the operating system is configured to determine a characteristic of the metal contamination in the semiconductor topography, and wherein the characteristic of the metal contamination in the semiconductor topography is a function of the measured electrical property of the semiconductor topography.

152. A computer-implemented method for controlling a system configured to determine a characteristic of metal contamination in a semiconductor topography, comprising:

controlling the system to anneal the semiconductor topography and to measure at least one electrical property of the semiconductor topography; and

determining the characteristic of the metal contamination in the semiconductor topography, wherein the characteristic of the metal contamination is a function of the measured electrical property of the semiconductor topography.

153. The method of claim 152, wherein the semiconductor topography comprises a semiconductor substrate.

154. The method of claim 152, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate.

155. The method of claim 152, wherein controlling the system to anneal the semiconductor topography comprises controlling the system to heat the semiconductor topography to an anneal temperature of less than approximately 1100 °C.

156. The method of claim 152, wherein the semiconductor topography comprises a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the semiconductor substrate.

157. The method of claim 152, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the dielectric material.

158. The method of claim 152, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on an upper surface of the semiconductor topography.

159. The method of claim 152, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on predetermined regions of the semiconductor topography.

160. The method of claim 152, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on a portion of the semiconductor topography or on substantially the entire semiconductor topography.

161. The method of claim 152, wherein the system comprises a non-contact work function sensor, and wherein controlling the system to measure the electrical property of the semiconductor topography comprises controlling the sensor.

162. The method of claim 152, wherein the system comprises a movable chuck, and wherein controlling the system comprises controlling the movable chuck to alter a position of the semiconductor topography under a non-contact corona charging device.

163. The method of claim 152, wherein the system further comprises a robotic wafer handler, and wherein controlling the system comprises controlling the robotic wafer handler to move the semiconductor topography.

164. The method of claim 152, wherein the system further comprises a pre-aligner, and wherein controlling the system comprises controlling the pre-aligner to alter a position of the semiconductor topography.

165. The method of claim 152, wherein the system further comprises a cooling device, wherein controlling the system comprises controlling the cooling device to reduce a temperature of the semiconductor topography subsequent to annealing the semiconductor topography.

166. The method of claim 152, wherein the electrical property of the semiconductor topography comprises a tunneling voltage.

167. The method of claim 152, wherein the electrical property of the semiconductor topography comprises a surface voltage.

168. The method of claim 152, wherein the electrical property of the semiconductor topography comprises a surface voltage, and wherein the surface voltage is a function of time.

169. The method of claim 152, wherein the electrical property of the semiconductor topography comprises a surface photo-voltage of the semiconductor topography, and wherein the system further comprises an illumination system and a movable chuck, and wherein controlling the system comprises controlling the illumination system to direct a pulse of light toward the semiconductor substrate and controlling the movable chuck to alter a position of the semiconductor topography under the illumination system.

170. A system comprising:

a system configured to determine a characteristic of metal contamination in a semiconductor topography;

a controller computer coupled to the system; and

controller software executable on the controller computer, wherein the controller software is operable to implement a method for controlling the system, the method comprising:

controlling the system to anneal the semiconductor topography and to measure at least one electrical property of the semiconductor topography; and

determining a characteristic of the metal contamination in the semiconductor topography, wherein the characteristic of the metal contamination is a function of the measured electrical property of the semiconductor topography.

171. The system of claim 170, wherein the semiconductor topography comprises a semiconductor substrate.

172. The system of claim 170, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate.

173. The system of claim 170, wherein controlling the system to anneal the semiconductor topography comprises controlling the system to heat the semiconductor topography to an anneal temperature of less than approximately 1100 °C.

174. The system of claim 170, wherein the semiconductor topography comprises a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the semiconductor substrate.

175. The system of claim 170, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the dielectric material.

176. The system of claim 170, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on an upper surface of the semiconductor topography.

177. The system of claim 170, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on predetermined regions of the semiconductor topography.

178. The system of claim 170, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on a portion of the semiconductor topography or on substantially the entire semiconductor topography.

179. The system of claim 170, wherein the system comprises a non-contact work function sensor, and wherein controlling the system to measure the electrical property of the semiconductor topography comprises controlling the sensor.

180. The system of claim 170, wherein the system comprises a movable chuck, and wherein controlling the system comprises controlling the movable chuck to alter a position of the semiconductor topography under a non-contact corona charging device.

181. The system of claim 170, wherein the system further comprises a robotic wafer

handler, and wherein controlling the system comprises controlling the robotic wafer handler to move the semiconductor topography.

182. The system of claim 170, wherein the system further comprises a pre-aligner, and wherein controlling the system comprises controlling the pre-aligner to alter a position of the semiconductor topography.

183. The system of claim 170, wherein the system further comprises a cooling device, wherein controlling the system comprises controlling the cooling device to reduce a temperature of the semiconductor topography subsequent to annealing the semiconductor topography.

184. The system of claim 170, wherein the electrical property of the semiconductor topography comprises a tunneling voltage.

185. The system of claim 170, wherein the electrical property of the semiconductor topography comprises a surface voltage.

186. The system of claim 170, wherein the electrical property of the semiconductor topography comprises a surface voltage, and wherein the surface voltage is a function of time.

187. The system of claim 170, wherein the electrical property of the semiconductor topography comprises a surface photo-voltage of the semiconductor topography, wherein the system further comprises an illumination system and a movable chuck, and wherein the controlling the system comprises controlling the illumination system to direct a pulse of light toward the semiconductor substrate and controlling the movable chuck to alter a position of the semiconductor topography under the illumination system.

188. A carrier medium comprising program instructions, wherein the program instructions are computer-executable to implement a method for controlling a system, and wherein the method comprises:

controlling the system to anneal a semiconductor topography and to measure at least one electrical property of the semiconductor topography; and

determining a characteristic of metal contamination in the semiconductor topography, wherein the characteristic of the metal contamination is a function of the measured electrical property of the semiconductor topography.

189. The carrier medium of claim 188, wherein the semiconductor topography comprises a semiconductor substrate.

190. The carrier medium of claim 188, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate.

191. The carrier medium of claim 188, wherein controlling the system to anneal the semiconductor topography comprises controlling the system to heat the semiconductor topography to an anneal temperature of less than approximately 1100 °C.

192. The carrier medium of claim 188, wherein the semiconductor topography comprises a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the semiconductor substrate.

193. The carrier medium of claim 188, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate, and wherein controlling the system to anneal the semiconductor topography is effective to drive the metal contamination into the dielectric material.

194. The carrier medium of claim 188, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on an upper surface of the semiconductor topography.

195. The carrier medium of claim 188, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on predetermined regions of the semiconductor topography.

196. The carrier medium of claim 188, wherein the system comprises a non-contact corona charging device, and wherein controlling the system comprises controlling the device to deposit a charge on a portion of the semiconductor topography or on substantially the entire semiconductor topography.

197. The carrier medium of claim 188, wherein the system comprises a non-contact work function sensor, and wherein controlling the system to measure the electrical property of the semiconductor topography comprises controlling the sensor.

198. The carrier medium of claim 188, wherein the system comprises a movable chuck, and wherein controlling the system comprises controlling the movable chuck to alter a position of the semiconductor topography under a non-contact corona charging device.

199. The carrier medium of claim 188, wherein the system further comprises a robotic

wafer handler, and wherein controlling the system comprises controlling the robotic wafer handler to move the semiconductor topography.

200. The carrier medium of claim 188, wherein the system further comprises a pre-aligner, and wherein controlling the system comprises controlling the pre-aligner to alter a position of the semiconductor topography.

201. The carrier medium of claim 188, wherein the system further comprises a cooling device, wherein controlling the system comprises controlling the cooling device to reduce a temperature of the semiconductor topography subsequent to annealing the semiconductor topography.

202. The carrier medium of claim 188, wherein the electrical property of the semiconductor topography comprises a tunneling voltage.

203. The carrier medium of claim 188, wherein the electrical property of the semiconductor topography comprises a surface voltage.

204. The carrier medium of claim 188, wherein the electrical property of the semiconductor topography comprises a surface voltage, and wherein the surface voltage is a function of time.

205. The carrier medium of claim 188, wherein the electrical property of the semiconductor topography comprises a surface photo-voltage of the semiconductor topography, wherein the system further comprises an illumination system and a movable chuck, and wherein the controlling the system comprises controlling the illumination system to direct a pulse of light toward the semiconductor substrate and controlling the

movable chuck to alter a position of the semiconductor topography under the illumination system.

206. A method for fabricating a semiconductor device, comprising:

annealing a semiconductor topography;

measuring at least one electrical property of the semiconductor topography;

determining a characteristic of metal contamination in the semiconductor topography, wherein the characteristic of the metal contamination is a function of the measured electrical property;

comparing the characteristic of the metal contamination in the semiconductor topography to a range of acceptable characteristics of the metal contamination; and

forming the semiconductor device on the semiconductor topography, if the characteristic of the metal contamination is within the range of acceptable characteristics.

207. The method of claim 206, wherein the semiconductor topography comprises a semiconductor substrate.

208. The method of claim 206, wherein the semiconductor topography comprises a dielectric material disposed upon a semiconductor substrate.

209. The method of claim 206, wherein the annealed semiconductor topography is substantially free of damage.

210. The method of claim 206, wherein annealing the semiconductor topography comprises heating the semiconductor topography to an annealing temperature, and wherein the metal contamination comprises one type of metal contamination.

211. The method of claim 206, wherein the metal contamination comprises at least two types of metal contamination.

212. The method of claim 206, wherein annealing the semiconductor topography comprises heating the semiconductor topography to an annealing temperature of less than approximately 1100 °C.

213. The method of claim 206, wherein the metal contamination comprises copper, and wherein annealing the semiconductor topography comprises heating the semiconductor topography to an annealing temperature of approximately 350 °C to approximately 500 °C.

214. The method of claim 206, wherein the metal contamination comprises copper, wherein annealing the semiconductor topography comprises heating the semiconductor topography for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes.

215. The method of claim 206, wherein measuring the electrical property comprises depositing a charge on an upper surface of the semiconductor topography, and wherein depositing the charge comprises using a non-contact corona charging technique.

216. The method of claim 206, wherein measuring the electrical property comprises depositing a charge on an upper surface of the semiconductor topography, and wherein depositing a charge on the upper surface of the semiconductor topography comprises depositing the charge on predetermined regions of the upper surface of the semiconductor topography.

217. The method of claim 206, wherein measuring the electrical property comprises depositing a charge on an upper surface of the semiconductor topography, and wherein depositing the charge on the upper surface of the semiconductor topography comprises depositing the charge on a portion of the upper surface or on substantially the entire upper surface.

218. The method of claim 206, wherein measuring the electrical property of the semiconductor topography comprises using a non-contact work function measurement technique.

219. The method of claim 206, further comprising comparing the electrical property of the semiconductor topography to an electrical property of a reference semiconductor topography, wherein the reference dielectric material is substantially free of metal contamination.

220. The method of claim 206, further comprising comparing the electrical property of the semiconductor topography to an electrical property of a reference semiconductor topography, wherein the reference semiconductor topography comprises a predetermined level of at least one type of metal contamination, and wherein at least the one type of metal contamination is predetermined.

221. The method of claim 220, further comprising determining a presence of at least one type of metal contamination in the semiconductor topography.

222. The method of claim 206, wherein the electrical property of the semiconductor topography comprises a tunneling voltage.

223. The method of claim 206, wherein the electrical property of the semiconductor topography comprises a surface voltage.

224. The method of claim 206, wherein the electrical property of the semiconductor topography comprises a surface voltage, and wherein the surface voltage is a function of time.

225. The method of claim 206, further comprising directing a pulse of light toward the semiconductor topography prior to measuring the electrical property, and wherein the electrical property of the semiconductor topography comprises a surface photo-voltage.

226. The method of claim 206, wherein the characteristic of the metal contamination is a function of a temperature of annealing the semiconductor topography.

227. The method of claim 206, wherein the characteristic of the metal contamination is a function of an amount of the deposited charge.

228. The method of claim 206, wherein determining the characteristic of the metal contamination in the semiconductor topography comprises determining a characteristic of at least two types of metal contamination in the semiconductor topography.

229. The method of claim 206, wherein determining a characteristic of the metal contamination in the semiconductor topography comprises determining a characteristic of at least one type of metal contamination in a portion of the semiconductor topography, and wherein the portion of the semiconductor topography comprises a locally contaminated region of the semiconductor topography.

230. The method of claim 206, further comprising measuring the electrical property of the semiconductor topography at more than one position on the semiconductor topography, and determining the characteristic of at least one type of metal contamination at each measurement position.

231. The method of claim 230, further comprising generating a plot of the measured electrical property as a function of measurement position.

232. The method of claim 231, further comprising comparing the generated plot of the measured electrical property as a function of measurement position to a plot of a predetermined electrical property as a function of measurement position.

233. The method of claim 232, wherein the predetermined electrical property is representative of a range of acceptable levels of at least one type of metal contamination, and wherein the acceptable levels of the metal contamination do not substantially hinder the performance of a semiconductor device formed on the semiconductor topography.

234. The method of claim 206, wherein the semiconductor topography comprises a dielectric material disposed upon the semiconductor substrate, and wherein the dielectric material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

235. The method of claim 206, wherein the semiconductor topography comprises a semiconductor substrate, and wherein the semiconductor substrate comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

236. The method of claim 206, wherein the metal contamination comprises copper.

237. The method of claim 206, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum.

238. The method of claim 206, further comprising comparing the electrical property to a set of data, wherein the set of data comprises electrical properties associated with a characteristic of metal contamination.

239. The method of claim 206, further comprising

re-annealing the semiconductor topography subsequent to measuring the electrical property; and

re-measuring the electrical property of the semiconductor topography.

240. The method of claim 206, wherein the range of acceptable characteristics of the metal contamination in the semiconductor topography comprises levels of the metal contamination which may not substantially hinder the performance of a semiconductor device, and wherein the semiconductor device is formed on the semiconductor topography.